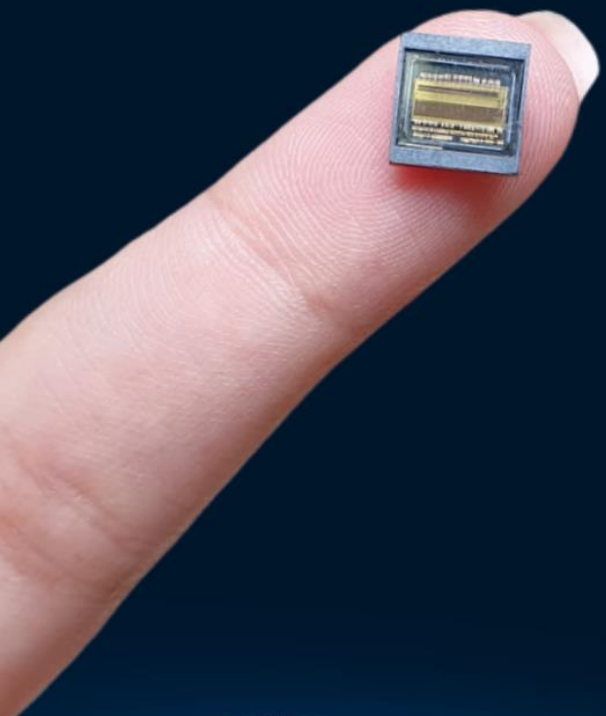
NEWSIGHT
IMAGING
WHERE TECHNOLOGY SHINES

3D Machine Vision

NSI1000

CMOS Image Sensor

1024 x 32 pixels



Supported by enhanced Time-of-Flight (eTOF™), the sensor is a perfect fit for applications such as Automotive safety, Robotics, Industry 4.0, LiDAR and more.

The NSI1000 is a CMOS image sensor for machine vision applications. It is designed for high volume markets such as robotics LiDAR, industry 4.0, automotive & ADAS and smart city markets, which require accurate high resolution in a competitive price. The sensor is composed of 32 rows of 1024 pixels, and two effective lines of 2048 pixels which are composed of analog binned pixels. One of these lines has larger pixels for added sensitivity and can also operate as one-line of 1024 pixels with ultra-high sensitivity.

The NSI1000 supports programmable frame rates, multiline triangulation, eTOF 3D distance measurement per pixel, automatic exposure control to avoid saturation from close or bright objects and enhance sensitivity to distant or dark objects, automatic peak detection for triangulation and per-frame configuration to allow on-the-fly reactions to events.

Features

The NSI1000 features a state-of-the-art global shutter array architecture, allowing extremely high sensitivity, while keeping low power dissipation.

Sensor Array Features

Array
- Matrix of 1024 x 32 global shutter and anti-blooming pixels, 4.8µm x 6µm

Lines
- 2 staggered rows, 1024 global shutter and anti-blooming pixels, 4.8µm x 10µm (2048 resolution)
- 2 staggered rows, 1024 pixels, 4.8µm x 16µm (2048 resolution) which can operate with analog binning as 1024 pixels of 9.6µm x 16µm

General Features

- Integrated configurable direct A/D converter with 8-10 bits precision
- Per-frame configuration and scenario scheduler
- Optional automatic exposure control
- Optional automatic triangulation peak detection per each line (center of mass algorithm support in HW)
- Solid state eTOF (Enhanced Time of Flight) support
- Multi-triangulation support, up to 32 concurrent vertical points (using a line laser)
- Integrated bandgap reference
- Integrated CDS for fixed-pattern noise reduction
- Output speed/ internal processing at up to 100 MHz
- Programmable frame rate up to
  - 3,125 fps – full array (1024 x 32)[1] [2]
  - 50,000 fps - high resolution triangulation line (2048)
  - 100,000 fps - low resolution high sensitivity triangulation line (1024)
- Optional shut down of frame clock (between frames) for reduced power consumption
- Optional data out inversion
- Double buffer mode for high frame rate

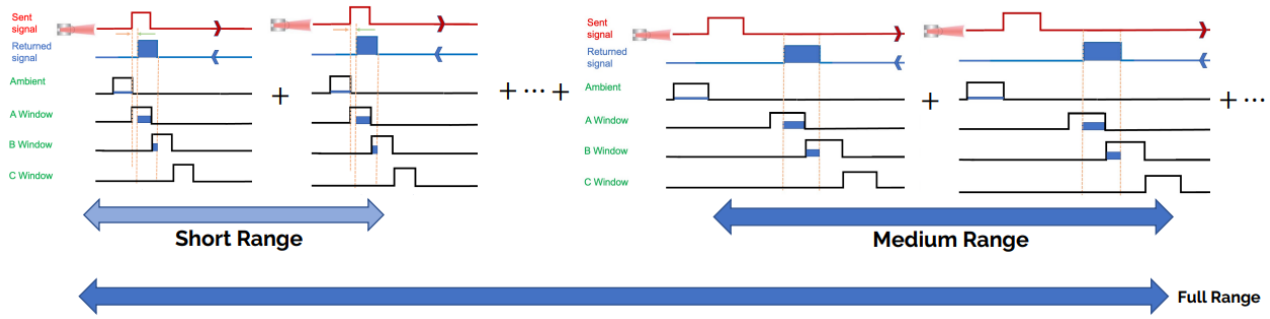
[1] In eTOF mode, the frame rate is reduced according to accumulation rate
[2] In “window of interest” mode the frame is increased in reverse ratio to the decrease of resolution

- Ambient light subtraction support
- Continuous or single frame capture modes
- Tristate data out pins for multiple parallel sensor connections

Applications

eTOF™ LiDAR

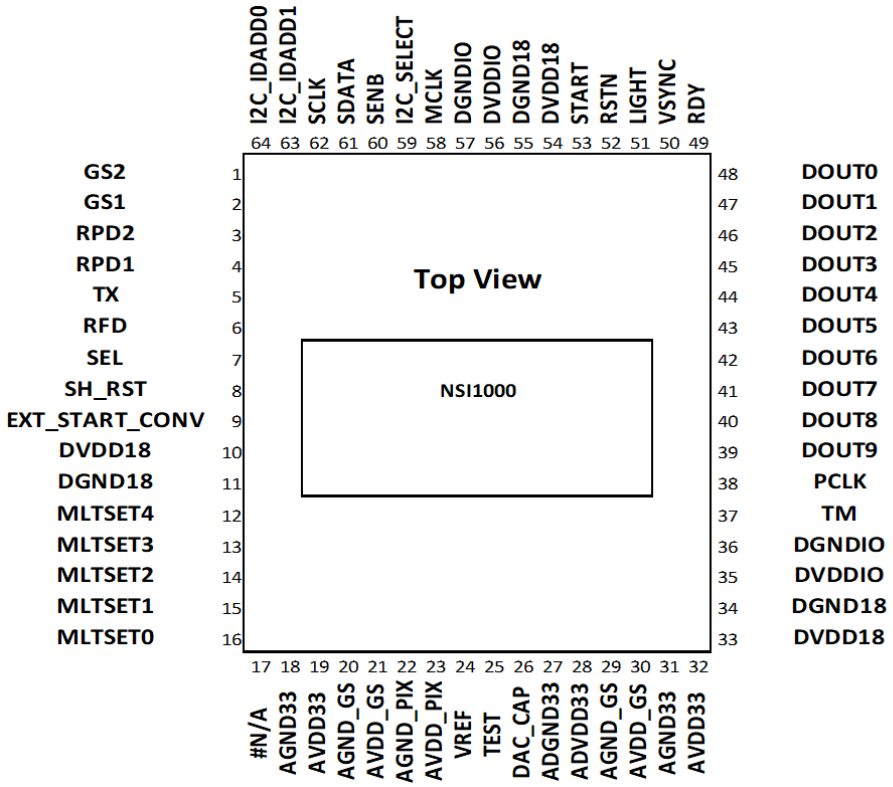
Newsight's eTOF™ (enhanced Time-of-Flight) is a patented solution for 3D distance measurement that allows unparalleled performance with less than a 1% error rate for distances up to 100m, both in indoor and outdoor scenarios. The eTOF™ solid-state LiDAR, based on the NSI1000, is a complete solution for a versatile and affordable 3D mapping device of 1024x32 points. Newsight offers a reference design which is highly configurable for different applications and very flexible in coping with different scenarios and environmental conditions.
The eTOF™ LiDAR is designed for a wide horizontal field of view (FOV) and a high frame rate. It provides high accuracy and precision with a high dynamic range.
The returned pulse can be sampled in 2, 3 or 4 windows. The diagram below illustrates one method of eTOF implementation using 3 sampling windows. Distance is calculated by the ratio of window A and window B, or window B and window C. Each frame accumulates charge from many sub-frames as many as 100K times, based on the accumulated exposure needed, to achieve optimal signal per distance and reflectivity.



Multi Triangulation LiDAR

Newsight Imaging's Multi Triangulation reference design offers a complete solution for versatile and affordable 3D scanning of 32 points. Newsight Imaging's Multi-Triangulation technology enables ultra-high accuracy for short-distance measurement applications. The technology supports a high frame rate and is highly configurable for different applications and scenarios.
Due to its high frame rate, Newsight Imaging's MT LiDAR can be a perfect solution for inspecting production lines.

Package and Pin Diagram



Pinout

Pins Description

Pin name	Pin no.	I/O	Signal type	Description
Power				
DVDD18	10,33,54	P	Power	Digital power supply (1.8 V)
DGND18	11,34,55	P	Power	Digital ground
DVDDIO	35,56	P	Power	Digital I/O power supply (3.3 V)
DGNDIO	36,57	P	Power	Digital I/O ground
AVDD33	19,32	P	Power	Analog power supply (3.3 V)
AGND33	18,31	P	Power	Analog ground
AVDD_GS	21,30	P	Power	Analog power supply Global Shutter (3.3V)
AGND_GS	20,29	P	Power	Analog Global Shutter ground
AVDD_PIX	23	P	Power	Analog Pixel power supply (3.3 V)
AGND_PIX	22	P	Power	Analog Pixel ground
ADVDD33	28	P	Power	Analog digital domain power supply (3.3 V)
ADGND33	27	P	Power	Analog digital domain ground

Pin name	Pin no.	I/O	Signal type	Description
Serial Interface				
I2C_SELECT	59	I	Control	Select I2C interface (high) or NSI1000 propriety serial interface (low)
I2C_IDADD0	64	I	Control	I2C base address (bit 0)
I2C_IDADD1	63	I	Control	I2C base address (bit 1)
SCLK	62	I	Control	Serial interface clock, used both for Newsight Imaging propriety serial interface and I2C interface
SDATA	61	I/O	Control	Serial interface data, synchronous to SCLK
SENB	60	I	Control	Serial interface enables, used only in case of Newsight Imaging proprietary serial interface. Synchronous to SCLK.
Control Inputs				
MCLK	58	I	Control	Master clock
RSTN	52	I	Control	Active low reset
START	53	I	Control	Start conversion signal (synchronized internally)
TM	37	I	Test	Tristate all output pins
Control Outputs				
LIGHT	51	O	Control	Light Illumination Pulse
Parallel Data Outputs				
PCLK	38	O	Control	Output data synchronized clock
RDY	49	O	Control	Parallel Data output row valid, synchronous to PCLK output rising edge.
VSYNC	50	O	Control	Parallel Data output frame valid, synchronous to PCLK output rising edge.
DOUT0	48	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT1	47	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT2	46	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT3	45	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT4	44	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT5	43	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT6	42	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT7	41	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
DOUT8	40	O	Digital	Digital output video data, synchronous to PCLK output rising edge.

Pin name	Pin no.	I/O	Signal type	Description
DOUT9	39	O	Digital	Digital output video data, synchronous to PCLK output rising edge.
Analog Test Pins				
DAC_CAP	26	A	Test	Ramp DAC cap input (should be connected to 1uF capacitor)
TEST	25	A	Test	Analog test pad
VREF	24	A	Test	Input for external DAC ramp, output of internal DAC ramp
Digital Test Pins				
GS2	1	I	Test	External control signal (for testing only)
GS1	2	I	Test	External control signal (for testing only)
RPD2	3	I	Test	External control signal (for testing only)
RPD1	4	I	Test	External control signal (for testing only)
TX	5	I	Test	External control signal (for testing only)
RFD	6	I	Test	External control signal (for testing only)
SEL	7	I	Test	External control signal (for testing only)
SH_RST	8	I	Test	External control signal (for testing only)
EXT_START_CONV	9	I	Test	External control signal (for testing only)
MLTSET4	12	I	Control	Multiset External Control bit 4
MLTSET3	13	I	Control	Multiset External Control bit 3
MLTSET2	14	I	Control	Multiset External Control bit 2
MLTSET1	15	I	Control	Multiset External Control bit 1
MLTSET0	16	I	Control	Multiset External Control bit 0

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Min	Max	Unit
DVDD18 – Digital power supply (1.8 V)	0	2.4	V
DVDDIO – Digital I/O power supply (3.3 V)	0	4.3	V
AVDD33 – Analog power supply (3.3 V)	0	4.3	V
AVDD_GS – Analog power supply Global Shutter (3.3V)	0	4.3	V
AVDD_PIX – Analog Pixel power supply (3.3 V)	0	4.3	V
ADVDD33 – Analog digital domain power supply (3.3 V)	0	4.3	V

Recommended Operating Conditions

Parameter	Min	Type	Max	Unit
DVDD18 – Digital power supply (1.8 V)	1.6	1.8	2.0	V
DVDDIO – Digital I/O power supply (3.3 V)	3.0	3.3	3.6	V

Parameter	Min	Type	Max	Unit
AVDD33 – Analog power supply (3.3 V)	3.0	3.3	3.6	V
AVDD_GS – Analog power supply Global Shutter (3.3V)	3.0	3.3	3.6	V
AVDD_PIX – Analog Pixel power supply (3.3 V)	3.0	3.3	3.6	V
ADVDD33 – Analog digital domain power supply (3.3 V)	3.0	3.3	3.6	V
Vih – High level input voltage	2.0			V
Vil – Low level input voltage			0.8	V
Voh (DVDDIO = 3.3v)		2.4	3.9	V
Vol (DVDDIO = 3.3v)	-0.3	0.4		V
P – Typical Power consumption @ 100MHZ		450		mW
Ta – Operating temperature	-20		80	Deg C
Ts – Storage temperature	-40		125	Deg C

Timing Characteristics

Parameter	Min	Type	Max	Unit
MCLK – Operating frequency			100	MHz
SCLK – Serial input clock frequency	MCLK/8			MHz
SDATA, SENB setup time (before SCLK)			4	ns
SDATA, SENB hold time (after SCLK)	0.5			ns
SDATA delay (after SCLK)	4			ns
DOUT delay (after PCLK)	3			ns
RDY delay (after PCLK)	3			ns
VSYNC delay (after PCLK)	3			ns

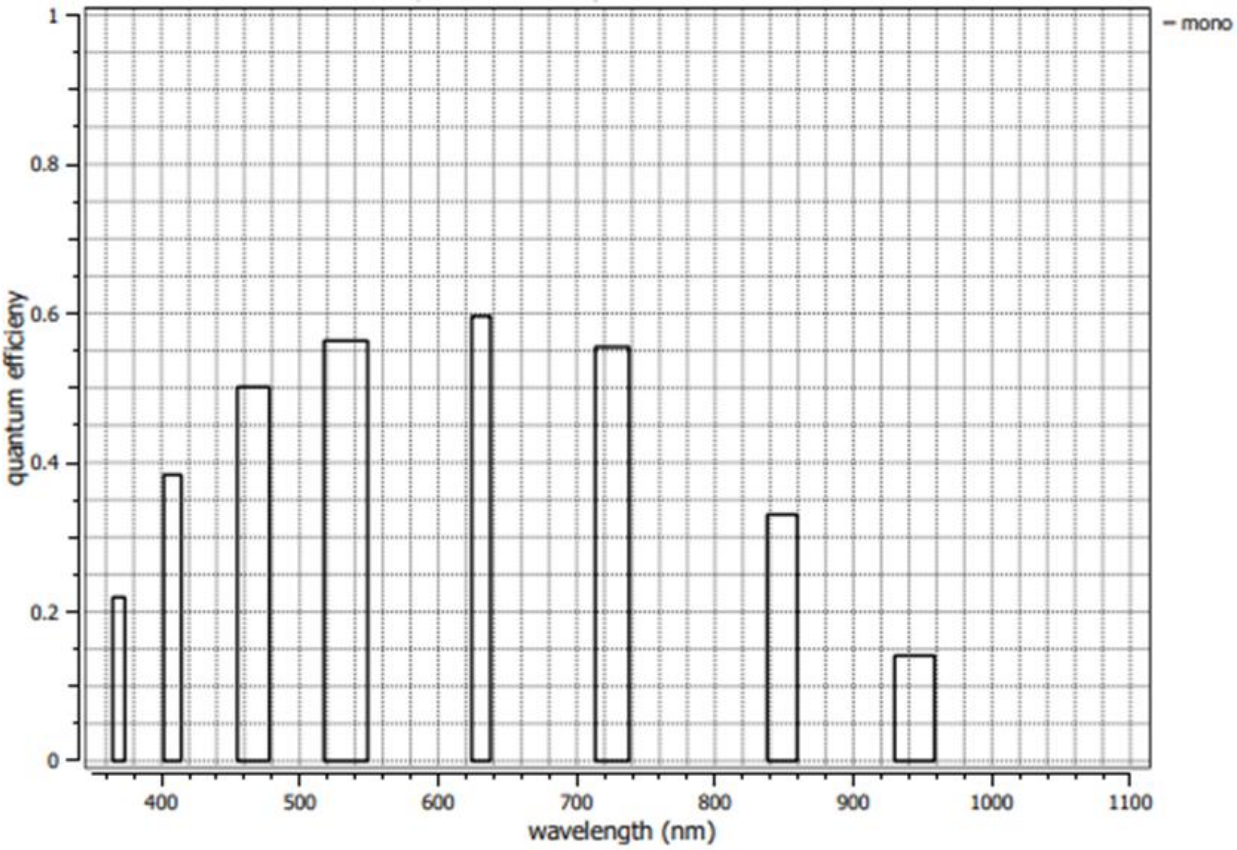
Optical and Sensor Characteristics

Pixel & Image Array Characteristics

Pixel characteristics are in accordance with the EMVA 1288 Linear standard, @ 850nm, 20C.

Parameter	Min	Type	Max	Unit
Pixel pitch		4.8 x 6		µm (x,y)
Array # of pixels		1024 x 32 (x,y)		
Array Size		4.915 x 0.192		mm
Quantum Efficiency @ 850nm		33.0		%
Quantum Efficiency @ 940nm		14.1		%
Pixel dark noise		21.6		e-
Dark current		11		ke-/s
Full well capacity		13.8		ke-
Conversion gain		0.04		DN/e-
Phase drift over temperature3		0.046		deg/°C

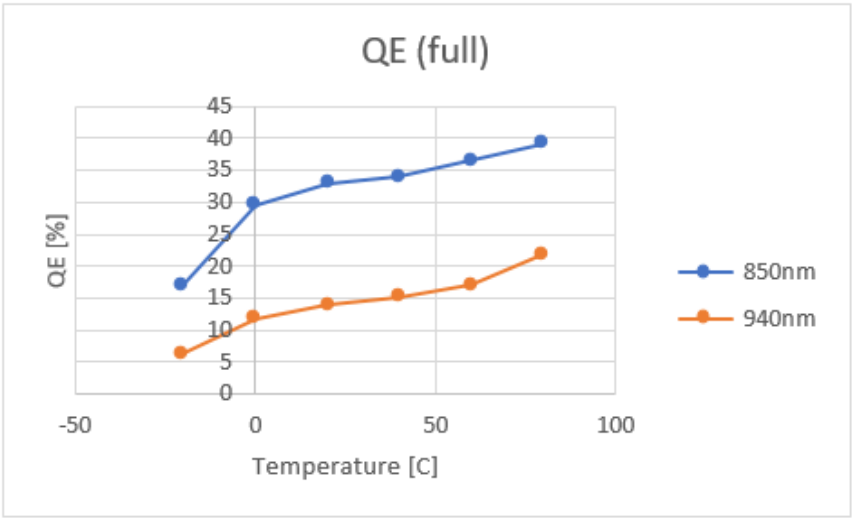
Parameter	Min	Type	Max	Unit
PRNU		1.55		%
DSNU		27		e-
Microlense(s)		Yes		
Maximum CRA (chief ray angle)		0		deg

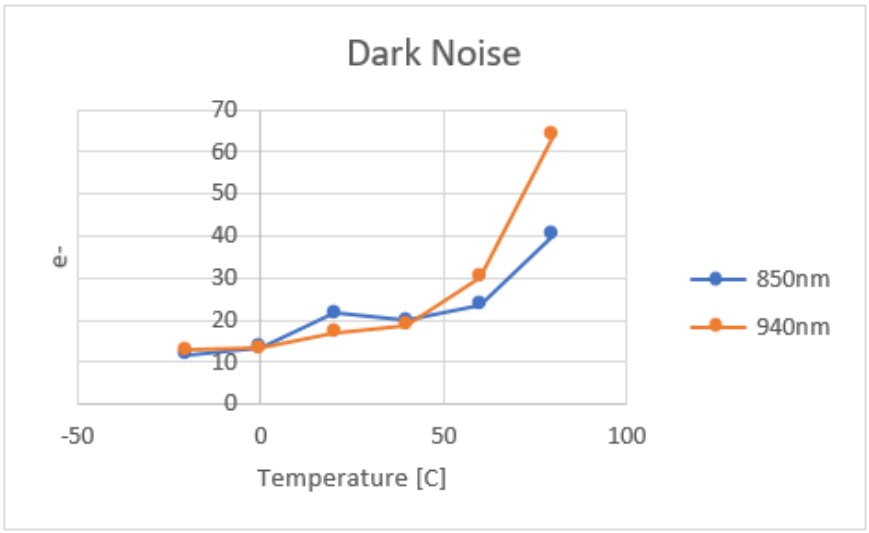


External Quantum Efficiency as a function of Wavelength

Performance over Temperature

NSI1000 performance at 850nm and 940nm wavelengths (NIR) over various temperatures in accordance with the 1288 Linear testing standard.



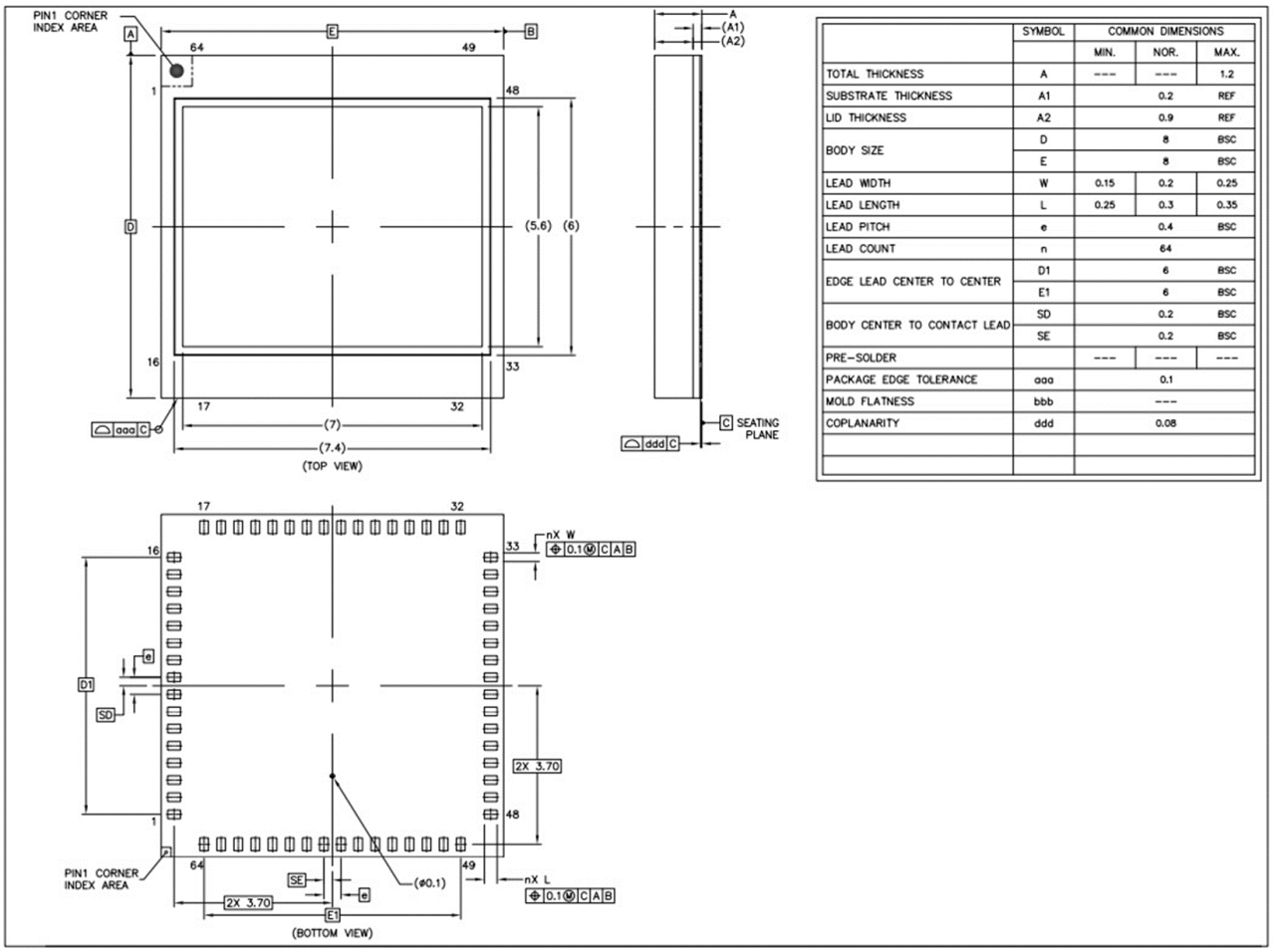


Optical Design Guidelines

- For good signal conditions it is recommended to use a passband filter incorporated into the camera optics. This helps block ambient sunlight from entering the sensor. Filter properties depend on the light source type and properties.
- For best power collection efficiency and hence overall power consumption it is recommended to use a lens with the lowest possible f-number.
- To enhance collection efficiency, the NSI1000M contains a micro-lens array with CRA = 0 deg. It would therefore be best to use a lens with a corresponding CRA = 0. Although a lens with higher CRA can work as well, the effect of a mismatch in CRA between lens and sensor reduces sensitivity towards array edges in the long sensor axis. The sensor's CRA may be customized to fit customer requirements at Newsight Imaging's discretion.

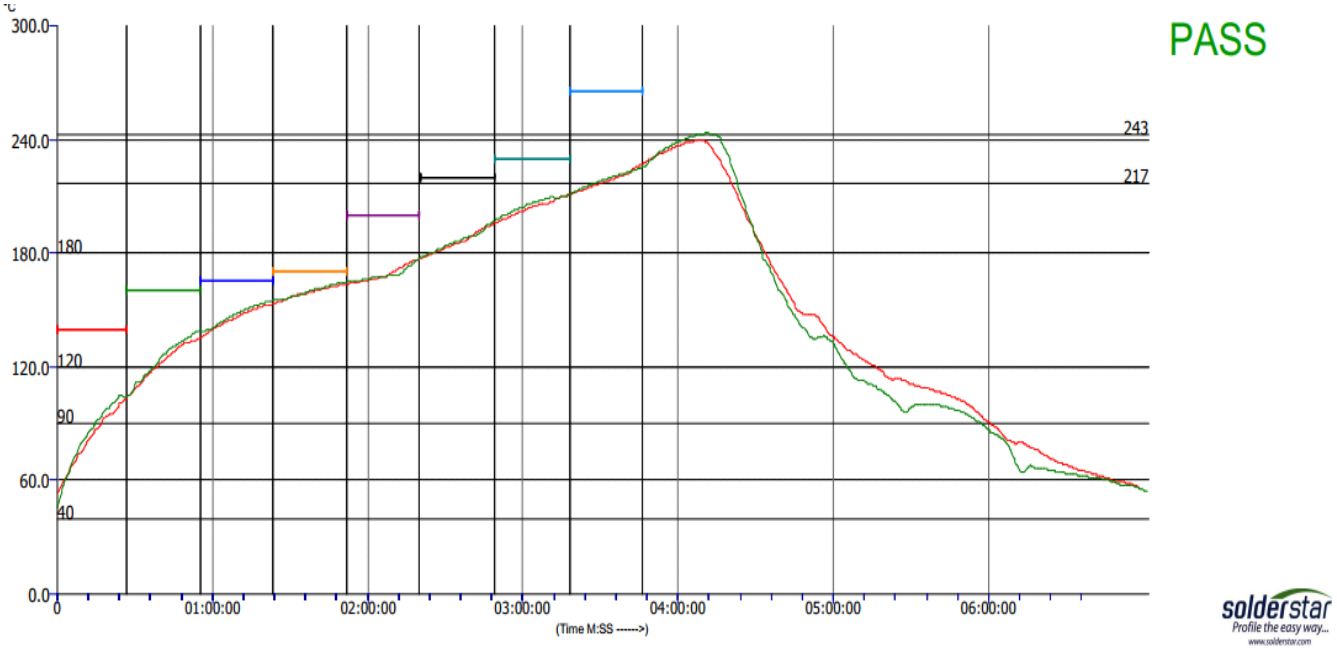
Package Description

NSI1000 Mechanical Dimensions



	SYMBOL	COMMON DIMENSIONS		
		MIN.	NOR.	MAX.
TOTAL THICKNESS	A	---	---	1.2
SUBSTRATE THICKNESS	A1		0.2	REF
LID THICKNESS	A2		0.9	REF
BODY SIZE	D		8	BSC
	E		8	BSC
LEAD WIDTH	W	0.15	0.2	0.25
LEAD LENGTH	L	0.25	0.3	0.35
LEAD PITCH	e		0.4	BSC
LEAD COUNT	n		64	
EDGE LEAD CENTER TO CENTER	D1		6	BSC
	E1		6	BSC
BODY CENTER TO CONTACT LEAD	SD		0.2	BSC
	SE		0.2	BSC
PRE-SOLDER		---	---	---
PACKAGE EDGE TOLERANCE	aaa		0.1	
MOLD FLATNESS	bbb		---	
COPLANARITY	ddd		0.08	

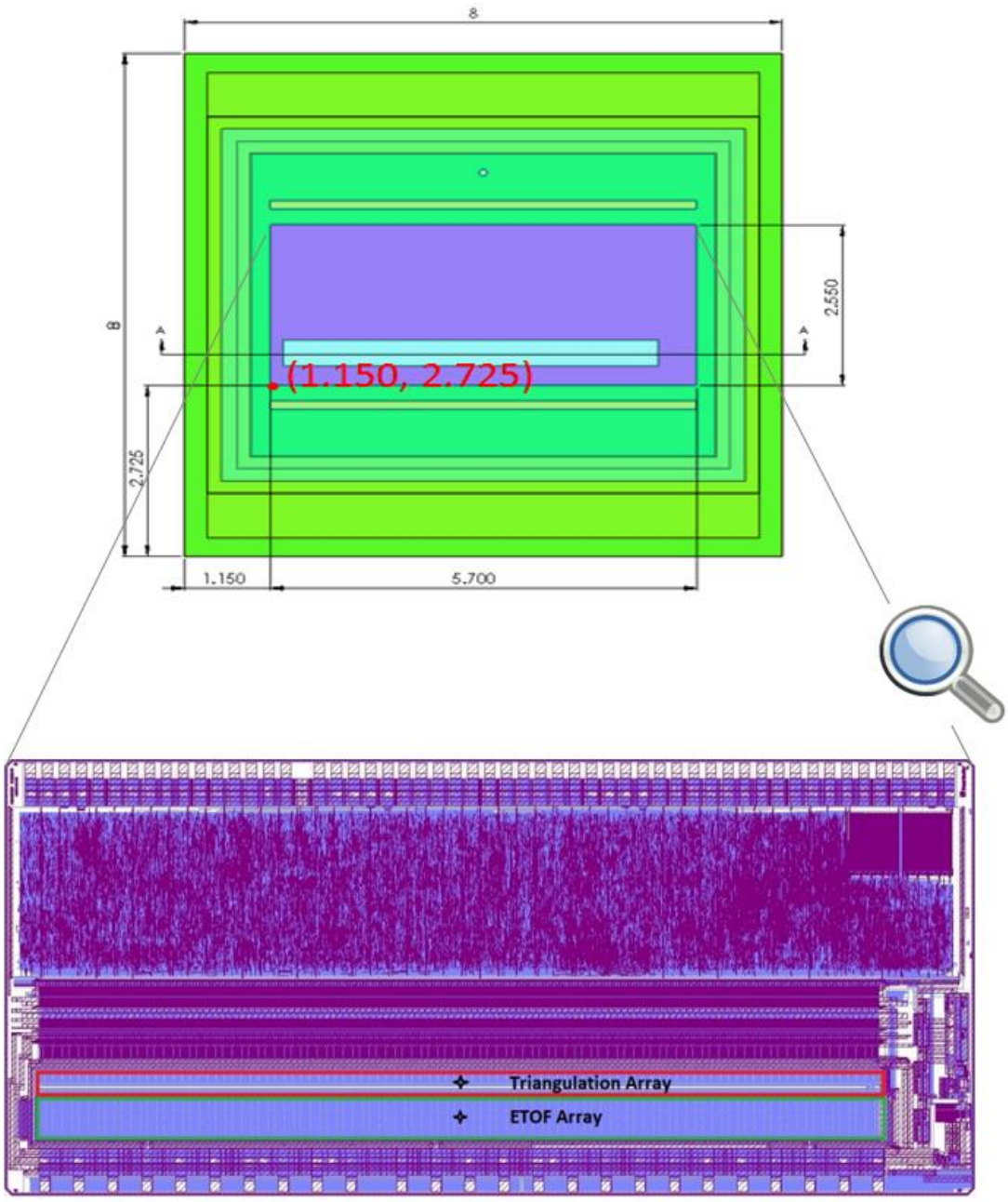
NSI1000 Solder Profile



NSI1000 Pixel Array Location – Package 8X8 mm

Die size: 5700 x 2550 µm

NSI1000 Location on Package



NSI1000 Location relative to lower left of package *	X (µm)	Y (µm)
Lower left	1150.0	2725.0
Upper right	6850.0	5275.0

* Tolerance: ± 100 µm

Triangulation Array

Array size: 4933.0 x 108.0 µm

Triangulation array relative to lower left of die	X (µm)	Y (µm)
Lower left	207.0	601.0
Upper right	5140.0	709.0
Center Point*	2673.5	655.0

* Tolerance: ± 100um

Triangulation array relative to lower left of package	X (µm)	Y (µm)
Lower left	1357.0	3326.0
Upper right	6290.0	3434.0
Center Point*	3823.5	3380.0

* Tolerance: ± 100um

eTOF Array

Array size: 4933.0 x 209.0 µm

Triangulation array relative to lower left of die	X (µm)	Y (µm)
Lower left	207.0	348.0
Upper right	5140.0	557.0
Center Point*	2673.5	452.5

* Tolerance: ± 100um

Triangulation array relative to lower left of package	X (µ m)	Y (µm)
Lower left	1357.0	3073.0
Upper right	6290.0	3282.0
Center Point*	3823.5	3177.5

* Tolerance: ± 100um

Serial Interface

The serial interface is used for programming the NSI1000 device and setting up the operational modes and the timing of the internal pixel control signals. The serial interface also allows reading the NSI1000 configuration. When the “I2C_SELECT” pin is driven low, the chosen protocol will be the synchronous serial interface which uses 3 signals: SCLK, SDATA and SENB.

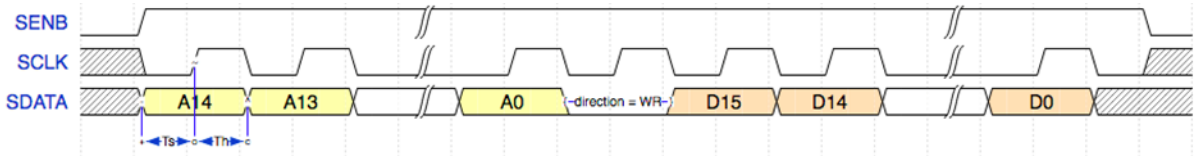
Serial Interface Signals

Signal name	Direction	Description
SENB	IN	Serial Enable: This signal must be asserted for the serial interface to function. The signal allows several NSI1000 devices to share the same SCLK and SDATA lines.
SCLK	IN	Serial interface clock signal
SDATA	IN/OUT	Bidirectional serial address and data line synchronous to SCLK

The protocol uses frames of 32 bits, 15 address bits, one direction bit and 16 data bits. The SDATA signal is sampled and driven by the NSI1000 device on the rising edge of the SCLK signal.

Serial Interface – Write Operation

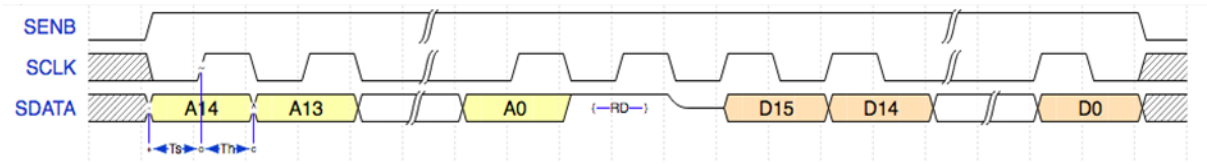
A write operation starts with driving SENB high. 15 bits of address are sent to the NSI1000 on the SDATA line, MSB first. Direction bit "0", indicating a write operation, follows the address bits. 16 bits of data are sent to the NSI1000 device, MSB first. When SENB is asserted low, the transfer ends.
If SENB goes low in the middle of a transfer, the transfer is terminated and ignored.
Data is latched in the NSI1000 interface on the rising edges of SCLK, so good practice is to drive the data using the falling edges of SCLK.



Serial Interface Write Transaction

Serial Interface – Read Operation

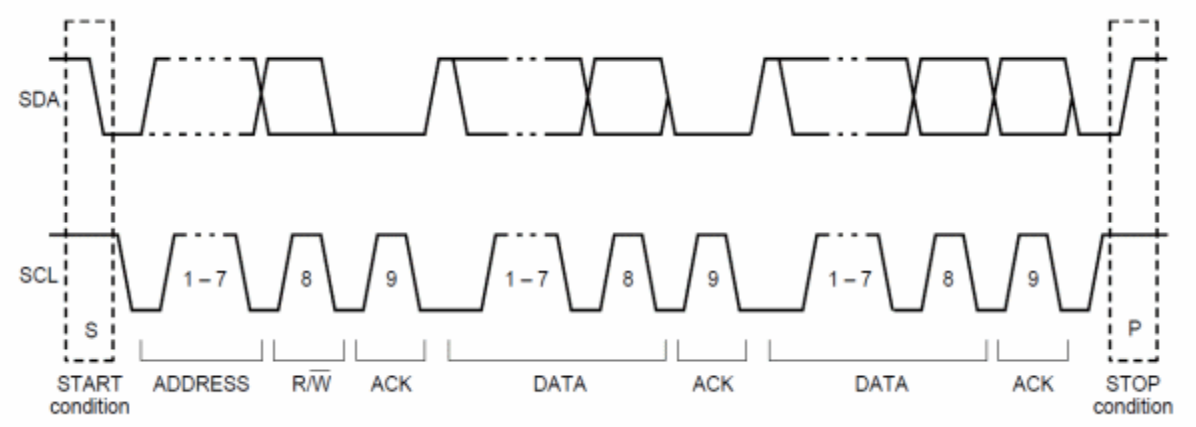
A read operation starts with driving SENB high. 15 bits of address are sent to the NSI1000 on the SDATA line, MSB first. Direction bit "1", indicating a read operation, follows the address bits. The driver releases the SDATA signal, to allow the NSI1000 device to drive the data out of the device. 16 bits of data are read from the NSI1000 device. When SENB is asserted low, the transfer ends.
If SENB goes low in the middle of a transfer, the transfer is terminated and ignored.
Data is driven by the NSI1000 interface on the rising edges of SCLK, so good practice is to sample the data externally using the falling edges of SCLK.



Serial Interface Read Transaction

Enhanced I²C Interface

The I2C bus protocol was invented in 1982 by Philips Semiconductor, and later enhanced by Texas Instruments. The I2C bus protocol is a Multi-Master/Multi-Slave serial bus, widely used for connecting low speed peripherals to processors and MCUs. The packet size of a standard I2C is 7-bits for address and 8-bits for data, as follows:



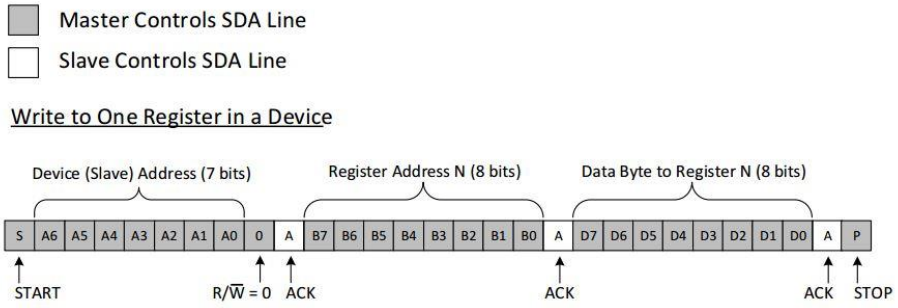
A complete I2C data transfer (courtesy of NXP semiconductors)

The NSI1000 registers can be configured using the enhanced I2C bus protocol. When the "I2C_SELECT" pin is driven high, the chosen protocol will be the I2C, and the "SCLK" and "SDATA" pins will be used to configure the chip.
The I2C implemented in NSI1000 supports only the enhanced 16-bit data and addresses, by using an encapsulation protocol over the standard I2C.
In order to support up to four NSI1000 chips on the I2C bus, the NS1000 I2C block can be configured to 4 different addresses according to the two input address pins:

I2C_IDADD0	I2C_IDADD1	DEVICE ADD
0	0	0x03C
1	0	0x03D
0	1	0x03E
1	1	0x03F

Standard I2C Write Transaction

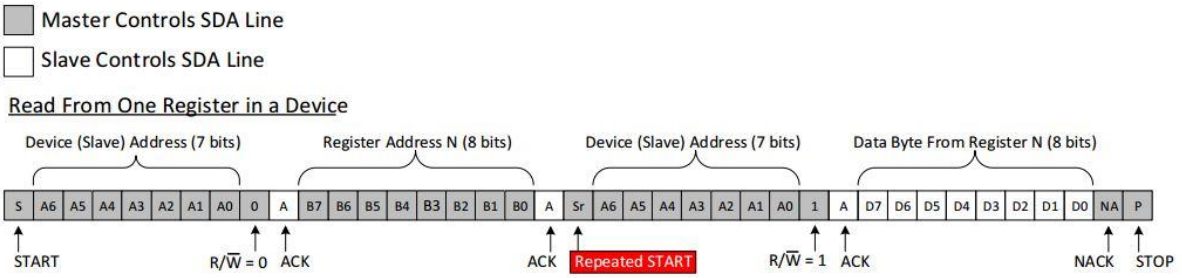
The master sends a "start" bit followed by the slave address and a "write" bit ("0"). After receiving an ACK from the slave, the master sends an 8-bit register address. After receiving an ACK from the slave, the master sends the 8-bit data to be written to the register. This transaction can continue with more write operations. The slave increments the address for each data byte received. The sequence ends with the master sending a "stop" bit.



Write transaction to a device register (courtesy of Texas Instruments)

Standard I2C Read Transaction

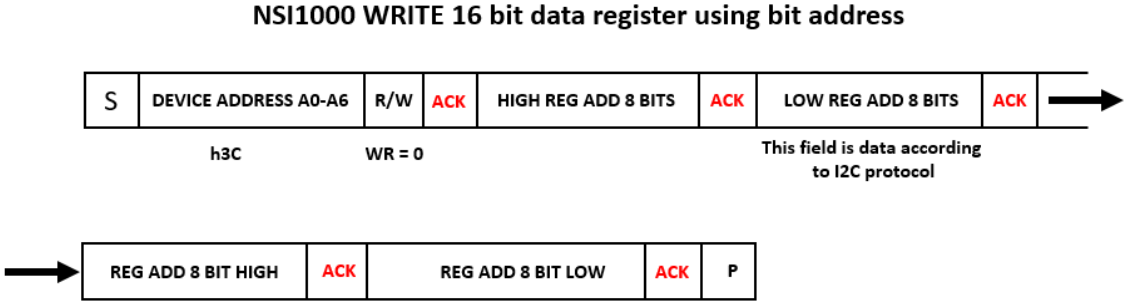
The master sends a "start" bit followed by the slave address and a "write" bit ("0"). After receiving an ACK from the slave, the master sends an 8-bit register address. After receiving an ACK from the slave, the master sends again a "start" bit followed by the slave address and a "read" bit ("1"). The slave sends the 8-bit data from the register. This transaction can continue with more read operations. The slave increments the address for each data byte transmitted. The sequence ends with the master sending a "NACK" + "stop" bit.



Read transaction from a device register (courtesy of Texas Instruments)

Enhanced I2C Write Transaction

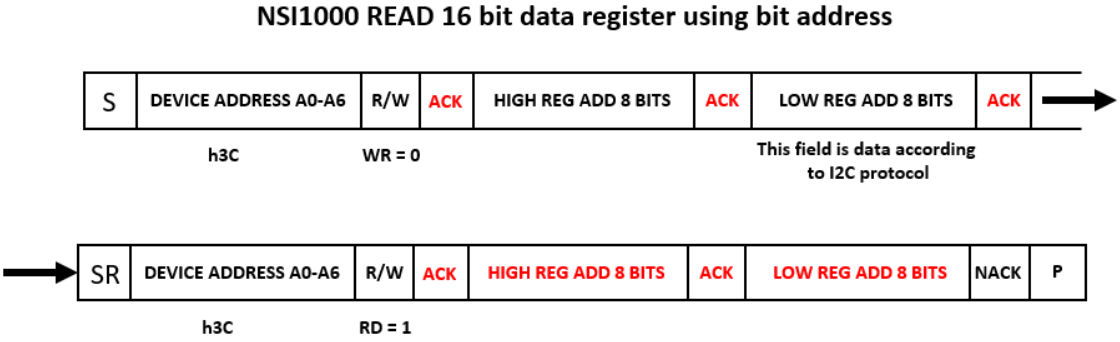
The master sends a "start" bit followed by the NSI1000 address and a "write" bit ("0"). After receiving an ACK from the chip, the master sends the *upper* 8-bit address of the register. After receiving an ACK from the chip, the master – instead of sending the 8-bit data to be written to the register – sends the *lower* 8-bit address of the register, followed by two 8-bit data write transactions.



Enhanced 16-bit write transaction to a sensor register

Enhanced I2C Read Transaction

The master sends a “start” bit followed by the NSI1000 address and a “write” bit (“0”). After receiving an ACK from the chip, the master sends the *upper* 8-bit address of the register. After receiving an ACK from the chip, the master sends the *lower* 8-bit address of the register. The master sends again a “start” bit followed by the chip address and a “read” bit (“1”). The chip sends the upper 8-bit data from the addressed register, followed by the lower 8-bit data. The sequence ends with the master sending a “NACK” + “stop” bit.



Enhanced 16-bit read transaction from a sensor register

Parallel Output Interface

Basic Timing (data only)

The data from the NSI1000 is driven out of the chip on DOUT pads. There are 10 data pads DOUT9-DOUT0. The number of valid data bits is a result of the DAC accuracy selected and can range from 8 to 10 bits. In all cases the data is aligned to the left always using the MSB pads. The data is valid when RDY is active and is driven out with the rising edge of PCLK. The RDY signal acts as the horizontal sync signal and marks the beginning and the end of a single row. The VSYNC acts as the vertical sync signal and marks the beginning and the end of a full frame.

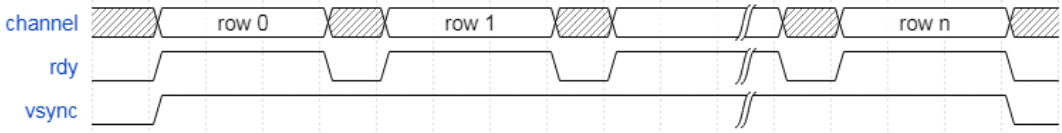


Figure 1 - Basic Timing for the RDY and VSYNC outputs during readout